REMARKS

The Examiner's Office Action dated December 4, 2002 has been received and its contents carefully noted. At the outset, Applicants note that the Examiner contends that the Information Disclosure Statement filed November 4, 2002 fails to comply with the provisions of 37 C.F.R. 1.97, 1.98 and MPEP § 609. A representative of the undersigned's firm held a telephone conference with Examiner B. Kebede regarding this issue, wherein the representative informed the Examiner that an Information Disclosure Statement was, in fact, not filed on this date. Upon reviewing the file history, the Examiner confirmed that an Information Disclosure Statement, indeed, was not filed. The Examiner's acknowledgement of consideration of the references disclosed in the Information Disclosure Statement of March 26, 2001 is appreciated.

Claims 1-60 were pending in the present application prior to the above amendment, of which claims 1-16 and 30-43 are withdrawn from consideration. By the above amendment, claims 17, 18, 44, 49, ,52 are amended. Accordingly, claims 1-60 remain pending, of which claims 17-29 and 44-60 are believed to be in condition for allowance for at least the following reasons.

A. 35 U.S.C. §112, 2nd Paragraph Rejection

Claims 52-60 stand rejected under 35 U.S.C. §112, 2nd paragraph as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Independent claim 52, in particular, is rejected on the basis that there is insufficient antecedent basis for the limitation "wherein **n** is an arbitrary number other than 0", in line 9.

Claim 52 is herein amended to replace the term "(1, -1, 0, 1)" with the term "(1, -1, 0, n)." As amended, claim 52 now contains sufficient antecedent basis for the limitation "wherein n is an arbitrary number other than 0". Accordingly, reconsideration and withdrawal of the rejection of claim 52 under 35 U.S.C. § 112, 2nd paragraph is respectfully requested.

Claims 53-60 are rejected as being dependent on the rejected independent claim 52. In view of the aforementioned amendment to claim 52, the rejection of claims 53-60 should also be reconsidered and withdrawn.

B. 35 U.S.C. §102 Rejection

Claims 17-29 and 44-60 stand rejected under 35 U.S.C. §102(e) as anticipated by U.S. Patent No. 6,335,546 to Tsuda et al. (Hereinafter "Tsuda"). Applicants respectfully contend that claimed invention as presently amended defines subject matter that is clearly patentably distinct over Tsuda for at least the reasons to follow.

As presently amended, the invention in accordance with claims 17, 18, and 49 is directed generally to a method for the manufacture of a semiconductor substrate including, *inter alia*, a step of preparing a substrate in which a surface thereof is formed a depression having a triangle or hexagonal figure when viewed from the substrate normal, and a step of forming on the surface of the substrate a semiconductor layer having a hexagonal structure, whereby the depression is filled by the semiconductor layer.

The invention in accordance with claim 44, as presently amended, is directed generally to a method for the manufacture of a semiconductor substrate including, *inter alia*, a step of preparing a substrate for crystal growth; a step of depositing on the crystal growth substrate a

first semiconductor layer having a hexagonal crystal structure; a step of exposing either a plane having a plane orientation of (1, -1, , 0, n) where the number n is an arbitrary number, or its equivalent plane by subjecting a part of the first semiconductor to an etching process; and after the exposing step, a step of depositing on the first semiconductor layer a second semiconductor layer having a hexagonal crystal structure, whereby the plane is covered with the second semiconductor layer.

As presently amended, the invention in accordance with claim 52 is directed to a method of manufacture of a semiconductor substrate including, *inter alia*, a step of forming a substrate having on a surface thereof a triangle or hexagonal projection, and a step of forming on the surface of the substrate a semiconductor layer having a hexagonal crystal structure, whereby said projection is capped with the semiconductor layer.

1. Tsuda et al. Fail to Teach the Claimed Invention

Applicants respectfully submit that Tsuda fails to expressly teach or inherently suggest each and every claim limitation set forth in independent claims 17, 18, 44, 49 and 52. For instance, with respect to the rejection of claims 17, 18, and 49, the Examiner contends that Tsuda discloses a step of preparing a substrate 400 in which a surface (i.e. GaN) therefore is formed a depression 403 having a triangle or hexagonal figure (See Fig. 9D) when viewed from the substrate normal. It is respectfully submitted, however, that contrary to the Examiner's contention, Figure 9D of Tsuda does not disclose this feature. That is, Tsuda does not disclose a substrate surface in which a surface therefore is formed a depression having a triangle or

hexagonal figure when viewed from the substrate normal. Rather, when viewed from the substrate normal, the depressions 403 of the semiconductor structure shown in Tsuda Fig. 9D have a rectangular figure, as illustrated in Fig. 9B of Tsuda.

Notwithstanding this deficiency, Tsuda also fails to disclose the step of forming on the surface of the substrate a semiconductor layer having a hexagonal crystal structure, whereby the depression is filled by the semiconductor layer, as recited in presently amended independent claims 17, 18, and 49. (See, e.g., Fig. 2B-2C and Fig. 6; Page 17, line 26 – Page 18, line 6). Accordingly, withdrawal of the rejection and allowance of claims 17, 18, and 49 are respectfully requested.

The aforementioned arguments set forth with respect to claims 7, 8, and 49, are applicable to claims 9-29 and 50, by virtue of being dependent on at least one of claims 7, 8 and 49. Accordingly, withdrawal of the rejections and allowance of dependent claims 9-29, 50, 55, and 59 are also respectfully requested.

With respect to the rejection of claim 44, Applicant respectfully submits that Tsuda, likewise, does not teach or suggest the step of forming on the surface of the substrate a semiconductor layer having a hexagonal crystal structure, whereby the plane is covered with the second semiconductor layer, as recited in presently amended claim 44. Accordingly, reconsideration and withdrawal of the rejection of independent claim 44 is requested.

Insomuch as the aforementioned arguments made with respect to independent claim 44 are applicable to dependent claims 45-48, reconsideration and withdrawal of the rejections of dependent claims 45-48 is also respectfully requested.

Finally, with respect to the rejection of claim 52, Applicants respectfully submit that Tsuda also does not disclose each and every claim limitation. As presently amended, claim 52 includes the step of forming on the surface of the substrate a semiconductor layer having a hexagonal crystal structure, whereby the projection is capped with the semiconductor layer. (See, e.g. Application Figs. 7, 8B, 8C; page 25, lines 22-25) As similarly discussed above with respect to the rejection of independent claims 7, 8, 44, and 49, Tsuda fails to disclose the feature "whereby the projection is capped with the second semiconductor layer". In view of the foregoing, it is clear that Tsuda does not teach or inherently suggest each and every limitation of claim 52. Accordingly, reconsideration and withdrawal of the rejections of independent claim 52 is requested.

Insomuch as the aforementioned arguments made with respect to independent claim 52 are applicable to dependent claims 53, 54, 56-58, and 60, reconsideration and withdrawal of the rejections of dependent claims 53, 54, 56-58, and 60 is respectfully requested.

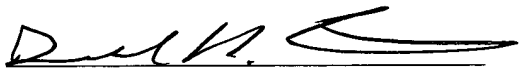
In view of the foregoing, it is respectfully submitted that Tsuda does not disclose each and every limitation of the rejected claims, as required for a case of anticipation under 35 U.S.C. § 102. Accordingly, withdrawal of the rejections of claims 17-29 and 44-60 is kindly requested.

Conclusion

Having responded to all rejections set forth in the outstanding Final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief

telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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MARKED UP VERSION

IN THE SPECIFICATION:

Please replace the last paragraph on page 22 of the application, starting with "Further, the figure", with the following corrected paragraph:

Further, the figure of the depression 104 when viewed from the substrate normal is not limited to an equilateral triangle. The figure of the depression 104 may be an equilateral hexagon. That is to say, as long as the figure of the depression 104 is a hexagon, the side faces of the depression 104 can be formed of {1, -1, 0, 1} planes, and the crystallinity of the side faces can be improved. In other words, since the side faces of the depression 104 can be (1, -1, 0, 1), (-1, 1, 0, 1), (0, 1, _1, 1), (0, -1, 1, 1), (-1, 0, 1, 1), and (1, 0, -1, 1), this makes it possible to improve the crystallinity of the side faces so as to improve the crystallinity of the second semiconductor layer 103 which crystal grows [form] from [al] at least the side faces. In such a case, the six angles of the hexagon that defines the outline of the depression 104 in the major surface of the first semiconductor layer 102 are, of course, all equal to 120 degrees.

IN THE CLAIMS:

Please amend claims 17, 18, 44, 49, and 52 as follows. Attached hereto is a marked-up copy of claims 17, 18, 44, 49, and 52 in their amended form.

17. (Twice Amended) A method for the manufacture of a semiconductor device comprising:

a step of preparing a substrate in which a surface thereof is formed a depression having a triangle or hexagonal figure when viewed from the substrate normal; and

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said depression is filled by said semiconductor layer,

wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n), where said number n is an arbitrary number other than 0, or its equivalent plane.

18. (Twice Amended) A method for the manufacture of a semiconductor device comprising:

a step of preparing a substrate;

a step of forming on a surface of said substrate a depression having a triangle or hexagonal figure when viewed from the substrate normal; and

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said depression is filled by said semiconductor layer,

wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane origination of (1, -1, 0, n), where said number n is an arbitrary number other than 0, or its equivalent plane.

44. (Amended) A method for the manufacture of a semiconductor substrate including:

a step of preparing a substrate for crystal growth;

a step of depositing on said crystal growth substrate a first semiconductor layer having a hexagonal crystal structure;

a step of exposing either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process; and

after said exposing step, a step of depositing on said first semiconductor layer a second semiconductor layer having a hexagonal crystal structure, whereby said plane is covered with said second semiconductor layer

49. (Twice Amended) A method for the manufacture of a semiconductor substrate comprising:

a step of forming a substrate having on a surface thereof a depression having a triangle or hexagonal figure when viewed from the substrate normal;

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said structure is filled by said semiconductor layer; and

a step of taking out said semiconductor layer by removal of said substrate,

wherein said depression has an inside face defined by either a plane having a plane orientation of (1, -1, 0, n), where said number n is an arbitrary number other than 0, or its equivalent plane.

52. (Twice Amended) A method for the manufacture of a semiconductor substrate comprising:[;]

a step of forming a substrate having on a surface thereof a triangle or hexagonal projection;

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said projection is capped with said semiconductor layer; and

a step of taking out said semiconductor layer by removal of said substrate,

wherein said projection has a side face defined by either a plane having a plane orientation of [(1, -1, 0, 1)] (1, -1, 0, n), wherein said number n is an arbitrary number other than 0, or its equivalent plane.